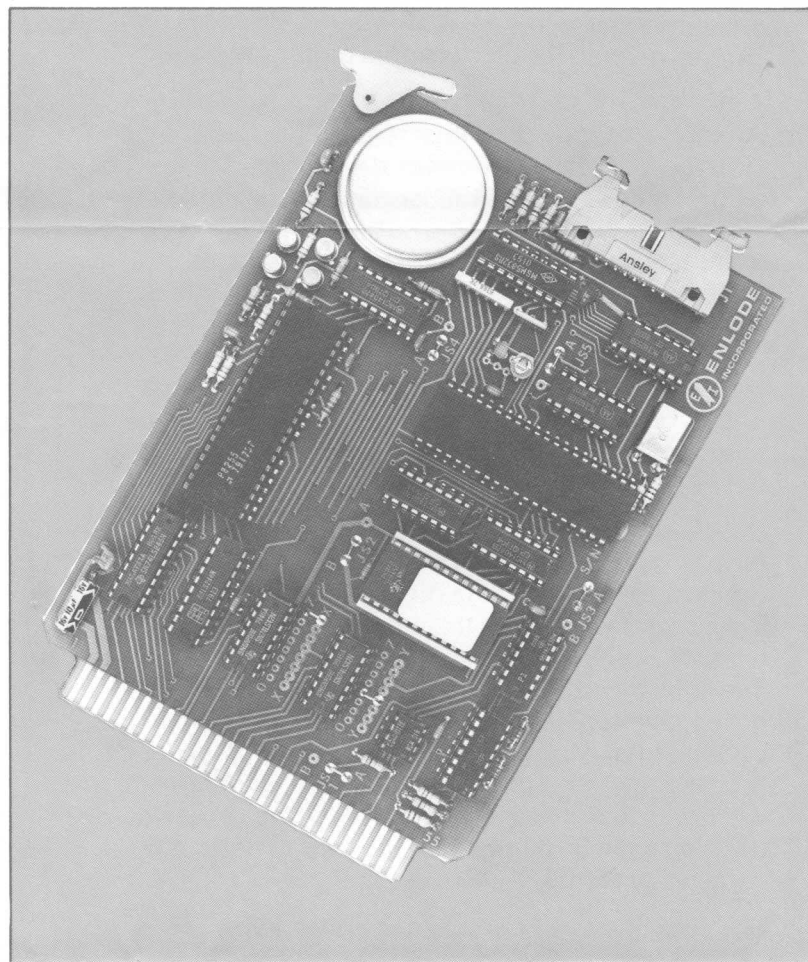


STD BUS

200-1

FEATURES

- Provides battery backed calendar and time data in years, months, days, day of week, hours, minutes, and seconds at ± 15 seconds per month accuracy.
- Programmable timer provides maskable or non-maskable interrupts in four ranges of 16 steps per range. Total range is 8.0 μ Sec through 512 seconds. Timed interrupt is usable in single or repeating modes by host processor command.
- Interrupt when preset time has been reached provides alarm clock function.
- On-board processor with separate ROM permits function modification for custom applications.
- Triple time-data buffers prevent 'split' data reads when clock time changes. No minimum timing restrictions on sequential reads.
- Host processor programmable vector call word may be changed at any time.
- Full hardware implementation of interrupt and priority chain signals may be disabled by board jumper or by host processor command.
- Auxiliary receptacle permits connection to remote display which will show time and date under clock card control. Host processor may over-ride for message display of 16 digits maximum. Time setting functions are accessible through receptacle connected switches or host processor control.
- 8085, 6800, and Z80 STD BUS compatible.
- Meets all STD BUS physical and electrical specifications.
- All I.C.'s socketed.



200-1 Clock and Interrupt Generator

APPLICATIONS

- Calendar/time-of-day data source.
- 'Stopwatch' timing measurement with sub-millisecond resolution and accuracy.
- 'Alarm clock' function for signal when specific time of day has been reached.
- Data source for panel display of time and date which requires no host processor overhead.

1728 Kingsley Avenue
 Orange Park, Florida 32073
 904-264-4405

GENERAL DESCRIPTION:

The 200-1 Clock/Interrupt Generator Card contains a crystal controlled clock chip which generates calendar and time-of-day data. This chip is powered by the +5V V_{CC} bus or an on-board lithium power cell. Continuous service life of this cell is in excess of three years and is extended when the clock card is powered by the V_{CC} bus.

An on-board processor interrogates the clock chip for calendar and time-of-day information in a burst mode every 65 milliseconds. This data is alternately loaded into two buffers. On host processor command, the most recently updated of these buffers is assigned for outputting data to the bus. The data contained within the "bus output" buffer remains constant until another register transfer command is received from the host processor. This permits the host to read any or all time data without any changes occurring between sequential reads.

Data is read from the card in single digit BCD format. The host processor must write to the card to select the desired data digit. The on-board processor then fetches this four-bit group and formats status bits in the upper four bit locations for output on the next read from the host processor. If the interrupt request signal is connected by strapping and the output port is programmed for interrupt generation, an interrupt will occur to signal the availability of the requested data; else the host must poll the card to determine data-ready status.

The card delivers hours data in either 12 or 24-hour format. Flags are used to indicate AM/PM, 12/24 format, and leap year.

An on-board programmable hardware timer can be set to deliver interrupts in 4 ranges: from 8 microseconds through 262 milliseconds, 2 milliseconds through 67 seconds, 61 microseconds through 2 seconds, or 15.6 milliseconds through

512 seconds. Each range contains 16 host processor selectable rates.

Selection of the range is by solder jumper on the card. This timer may be set to deliver one time interval and subsequently terminate until the next interval is commanded, or a continuing series of intervals. The rate may be changed at any time (within the solder jumper selected range) by host processor command. This interrupt may be identified from other interrupts by reading a status word.

The on-board processor may be commanded to generate a status word (with corresponding interrupt, if so programmed) when the clock time reaches a preset value. This function is limited to comparison of hours, minutes, and seconds.

The card I/O port may be programmed to deliver the 8085 and Z80 recognized vectors (C7 through FF) when the interrupt acknowledge bus line is activated.

The card has a 16 circuit receptacle (J1) located at the top edge to provide connection for a remote display and manual time-set pushbuttons. Pushbutton debounce is handled within the on-board processor. The receptacle carries four data lines, four address lines, one strobe line, two pushbutton control lines, and three +5V and two ground power lines. These circuits carry time data in HR-MN-SEC MO-DY-YR format.

A host processor command to the card will disable the time data output from J1 and will enable outputting host-processor-generated data to the display. Another host command returns the display output to time data.

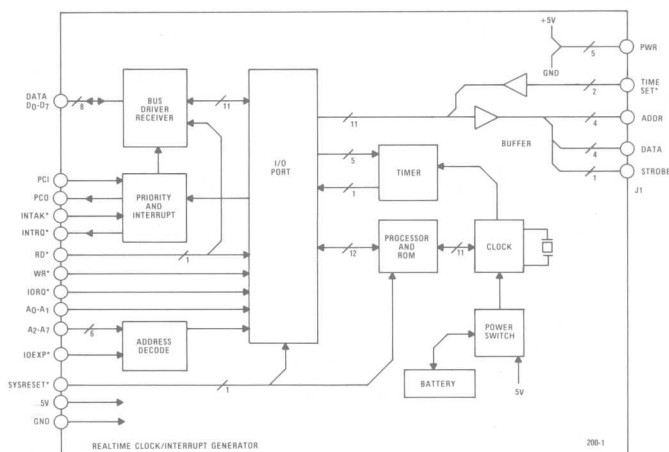
The card utilizes four sequential I/O mapped addresses. The six most significant address bits are decoded and may be jumper selected to locate the card anywhere within the 256 I/O address field.

SPECIFICATIONS:

ELECTRICAL SPECIFICATIONS

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
V _{CC}		4.5	5.0	5.5	Volts
I _{CC}			180	220	mA
Clock Oscillator			32.768	± 5PPm	kHz
Processor Oscillator			4.000	± .002%	MHz
<u>Display Signals</u>					
Data Valid Duration	*	52			uSec
Strobe Duration	*	8.0			uSec
I _{OL}	V _{OL} = 0.4, V _{CC} = 5.0	3.0			mA
I _{OH}	V _{OH} = 4.5, V _{CC} = 5.0	0.5			mA
Display I _{CC}				500	mA

*Data and address are stable for 40 uSeconds, minimum, before strobe and 4 uSeconds after strobe.



*Indicates active low signal.

200-1 EDGE CONNECTOR PIN LIST											
PIN NUMBER						PIN NUMBER					
OUTPUT (DRIVE)						OUTPUT (DRIVE)					
INPUT (LOADING)						INPUT (LOADING)					
mnemonic						mnemonic					
+5 VOLTS	VCC		2			1	VCC	+5 VOLTS			
GROUND	GND		4			3	GND	GROUND			
-5V			6			5		-5V			
D7		1	60	8		7	60	1	D3		
D6		1	60	10		9	60	1	D2		
D5		1	60	12		11	60	1	D1		
D4		1	60	14		13	60	1	D0		
A15				16		15		1	A7		
A14				18		17		1	A6		
A13				20		19		1	A5		
A12				22		21		1	A4		
A11				24		23		1	A3		
A10				26		25		1	A2		
A9				28		27		1	A1		
A8				30		29		1	A0		
RD*		1	32	31		31		1	WR*		
MEMRQ*				34		33		1	IORQ*		
MEMEX*				36		35		1	IOEXP*		
MCSYNC*				38		37			REFRESH*		
STATUS 0*				40		39			STATUS 1*		
BUSRQ*				42		41			BUSAK*		
INTRO*			60	44		43		1	INTAK*		
NMIRO*				46		45			WAITRQ*		
PBRESET*				48		47		1	SYSRESET*		
CNTRL*				50		49			CLOCK*		
PCI		1	52	51		51		5	PC0		
AUX GND				54		53			AUX GND		
AUX-V				56		55			AUX +V		

*DESIGNATES ACTIVE LOW LEVEL LOGIC

TIME DATA REGISTERS			
ITEM	RANGE	REGISTER	FLAGS
Seconds (units)	0-9	0	
Seconds (tens)	0-5	1	
Minutes (units)	0-9	2	
Minutes (tens)	0-5	3	
Hours (units)	0-9	4	
Hours (tens)	0-1/2	5	D2: 1 = PM D3: 1 = 24 hr D2: 0 = AM D3: 0 = 12 hr 0 = Sunday
Day of Week	0-6	6	
Day (units)	0-9	7	
Day (tens)	0-3	8	D2: 1 = Leap year
Month (units)	0-9	9	
Month (tens)	0-1	A	
Year (units)	0-9	B	
Year (tens)	0-9	C	

EXTERNAL INTERFACE - J1

*Mates with T&B Ansley #609-1630 or equivalent.

SOFTWARE, DOCUMENTATION and SCHEMATICS

*Software examples included in User's manual for 8085, Z80, and 6800 code.

*User's Manual documentation includes recommended display schematic.

ORDERING INFORMATION

*Realtime Clock/Programmable Interrupt Generator - Order #200-1.

200-1 CLOCK/INTERRUPT GENERATOR

Card Recognized Commands

and

Read Data Formats

DATA REGISTER

Card Address XXXX XX00

Commands (hex)

- 1N - Read Time Digit (N = digit)
- 20 - Exchange Time Buffer Registers
- 30 - Set Time Mode - 2 byte cmd
- (NM) - (N = digit, M = data)
- 40 - Display Control Mode/Stop Time
Display - multi byte cmd
- (NM) - (N = digit, M = data)
- 50 - Exit Display Control Mode
- 60 - Restart Time Display
- 70 - Set Compare-Time Mode - multi byte cmd
- (NM) - (N = digit, M = data)

Read Data Format

- D7 - Last Command Valid and Complete
- D6 - Time Comparison True
- D5 - Time Comparison Mode Active
- D4 - Pushbutton Time Set Active
- D3 - Data3
- D2 - Data2
- D1 - Data1
- D0 - Data0

- NOTES:**
1. Command execution time varies from 250 to 1000 microseconds in this register. Other registers response is immediate.
 2. Command completion must be verified by interrupt and/or status poll identification after every command byte written to the data register.
 3. Read from data register resets interrupt and status bit in status register.

TIMER/VECTOR REGISTER

Card Address XXXX XX01

Write Data Format

- D7 - Timer Rate3
- D6 - Timer Rate2
- D5 - Timer Rate1
- D4 - Timer Rate 0
- D3 - Timer Mode: Single/Repeat
- D2 - Vector Cmd2
- D1 - Vector Cmd1
- D0 - Vector Cmd0

Notes:

1. Timer rate code range: 0-F (hex)
2. Vector cmd range: 0-7 (hex) corresponds to RST0-RST7 vector call instructions.
3. Timer mode bit set 'single' causes timer to hold in reset when interval is complete.
4. Writing to this register will remove timer reset and initiate/continue interval.
5. Vector cmd and timer mode may be changed while timer interval is in progress.

STATUS REGISTER

Card Address XXXX XX10

Read Data Format

- D7 - Don't Care
- D6 - Don't Care
- D5 - Processor Cmd Complete
- D4 - Processor Interrupt Enabled
- D3 - Processor Interrupt Status
- D2 - Timer Interrupt Enabled
- D1 - Timer Interval Complete
- D0 - Timer Interrupt Status

Notes:

1. Processor interrupt and/or status bit are reset by reading data register.
2. Timer interrupt and/or status bit are reset by writing to timer/vector register. This action will initiate another interval if timer single mode is set.

CONTROL REGISTER

Card Address XXXX XX11

Commands (hex)

- C4 - Initialize
- 04 - Disable Timer Interrupt
- 05 - Enable Timer Interrupt
- 08 - Disable Processor Interrupt
- 09 - Enable Processor Interrupt

Notes:

1. C4 command must be written prior to any other card communication after power-up or system reset.

GENERAL NOTE: 1. Card address references define bits A1 and A0 which are fixed format. The upper six bits must correspond to I/O address mapping established by X and Y address strapping. Four sequential I/O addresses are used.